

AMENDMENTS TO THE CLAIMS

This Listing of Claims will replace all prior versions and listings of the Claims in the subject Patent Application:

Listing of Claims:

Claim 1 (Currently Amended): An integrated image detecting apparatus,
adopting ~~used~~ in CMOS process, comprising:

an optical detecting element ~~is operated to detect,~~ detecting an optical variation
and ~~convert photos~~ converting photons into charge;

an integrated integrator circuit ~~is operated to convert,~~ converting charge produced
by the optical detecting element into an electronic signal, wherein the integrator circuit
comprises a switch to control the voltage value of the electronic signal periodically in a
reset voltage, defined as a voltage when said switch is in an "on" condition, and in a
bright voltage, defined as a voltage when said switch is in an "off" condition, said reset
voltage and said bright voltage having differing values ~~that is a different type voltage~~;

a correlated double sampling circuit ~~connects,~~ connecting to the integrator circuit for
reading ~~read~~ the electronic signal of output from the integrated integrator circuit ~~output,~~
and generating an output signal with a voltage value of the difference between the reset
voltage and the bright voltage periodically following the operation of the switch of the

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~~integrator circuit for canceling variation of the optical detecting element and of the integrated circuit; and~~

an output circuit ~~performs,~~ receives the output signal of the correlated double sampling circuit and ~~output~~ outputs a plurality of signals.

Claim 2 (Currently Amended): The apparatus as claim 1, wherein the optical detecting element is a photodiode ~~adapted for both~~ adopting N-sub and or P-sub of CMOS process.

Claim 3 (Currently Amended): The apparatus as claim 1, wherein the ~~integrated integrator circuit~~ further comprises an operation operational amplifier connecting to the optical detecting element for receiving charge produced by the optical detecting element and outputting the electronic signal, a reference voltage, an electric charge storing device, a CMOS switch, and an inverter of CMOS., and the switch is connected between the input terminal and the output terminal of the operational amplifier which the switch is turned on and off periodically for controlling the voltage value of the electronic signal periodically in the reset voltage and in the bright voltage.

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Claim 4 (Currently Amended): The apparatus as claim 3, wherein the ~~operation~~ operational amplifier is a single stage amplifier ~~that consists~~ consisting of a plurality of NMOS or PMOS transistors, ~~and the reference voltage is an external voltage source or a bias provided by certain circuit inside, and the electric charge storing device is a capacitor, and the CMOS switch and the inverter of CMOS area~~ plurality of NMOS or PMOS transistors.

Claim 5 (Currently Amended): The apparatus as claim 1, wherein the correlated double sampling circuit ~~comprised~~ comprises an ac couple device, a CMOS switch, and a unit gain ~~operation~~ operational amplifier, the ac couple device is connected between the integrator circuit and the unit gain operational amplifier and the CMOS switch is connected between a reference voltage source and the transmission path of the ac couple device and the unit gain operational amplifier.

Claim 6 (Currently Amended): The apparatus as claim 5, wherein the ac couple device is a capacitor, ~~and the unit gain operation amplifier is a single stage amplifier that be substituted for a plurality of NMOS or PMOS transistors.~~

Claim 7 (Currently Amended): The apparatus as claim 1, wherein the output circuit comprises a sample and a hold circuit and a plurality of unit gain ~~operation~~ operational amplifiers.

Claim 8 (Currently Amended): The apparatus as claim 7, wherein the unit gain ~~operation~~ operational amplifier is a single stage amplifier ~~that consists~~ consisting of a plurality of NMOS or PMOS transistors.

Claim 9 (Currently Amended): The apparatus as claim 1, wherein ~~the different type voltage of the output signal for the integrated circuit further comprising:~~ the electronic signal is in the reset voltage while the switch inside the integrator circuit turns on, and the electronic signal is in the bright voltage while the switch inside the integrator circuit turns off ~~a reset voltage operated while switch turning on inside the integrated circuit; and a bright voltage operated while switch turning off inside the integrated circuit.~~

Claim 10 (Currently Amended): The apparatus as claim 9 1, wherein the switch is a transistor selected from the group consisting of ~~includes a~~ an NMOS transistor, a PMOS transistor, and a CMOS transistor ~~turned on at high voltage and turned off at low~~

~~voltage, and the switch is a PMOS transistor turned on at low voltage and turned off at high voltage, and the switch is a CMOS transistor turned on and turned off at both said high-low voltage.~~

Claim 11 (New): The apparatus as claim 3, wherein the charge storing device is a capacitor.

Claim 12 (New): The apparatus as claim 3, wherein the reference voltage is an external voltage source or a bias generated inside the ~~integrated~~ integrator circuit.

Claim 13 (New): The apparatus as claim 3, wherein the CMOS switch and the inverter of CMOS consists of a plurality of NMOS or PMOS transistors.

Claim 14 (New): The apparatus as claim 5, wherein the CMOS switch is turned on and off periodically corresponding to the switch of the ~~integrated~~ integrator circuit in order to conduct the reference voltage source and the ac couple device such that the ac couple device generates the output signal with a voltage value of the difference between the reset voltage and the bright voltage.

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Claim 15 (New): The apparatus of claim 14, wherein the CMOS switch of the correlated circuit turns on when the switch of the ~~integrated~~ integrator circuit is off, and the switch of the ~~integrated~~ integrator circuit turns on when the CMOS switch of the correlated circuit is off.

Claim 16 (New): The apparatus as claim 5, wherein the unit gain ~~operation~~ operational amplifier is a single stage amplifier consisting of a plurality of NMOS or PMOS transistors.